PATENT

Appl. No. 09/802,289
Amdt. dated July 21, 2004
Reply to Office Action of April 27, 2004

Amendments to the Abstract:

Please delete the entire abstract beginning on page 27, line 4, and replace the abstract with the following:

According to the invention, a processing core is disclosed. The processing core includes one or more processing pipelines and a number of register files. The processing pipelines having a total of N-number of processing paths, where each of the processing paths processes instructions on M-bit data words. Each of the number of register files has Q-number of registers that are each M-bits wide. The Q-number of registers within each of the plurality of register files are either private or global registers. When a value is written to one of said Q-number of said registers, which is a global register within one of said number of register files, the value is propagated to a corresponding global register in the other of the number of register files. When a value is written to one of said Q-number of the registers, which is a private register within one of said number of register files, the value is not propagated to a corresponding register in the other of said number of register files.